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William L. Betts
Paradyne Corporation
8545 126th Avenue, North
Largo, FL 33773

EXAMINER	
TORRES, JOSEPH D	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 08/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/777,213	BETTS, WILLIAM L.	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 May 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-77* is/are pending in the application.

4a) Of the above claim(s) *29,30,39-49 and 58-77* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28,31-38 and 50-57* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *29,30,39-49 and 58-77* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 February 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. 3.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

   I. Claims 1-28, 31-38 and 50-57 drawn to An Adaptive Interleaved Convolutional Encoder (Note: The Applicant originally elected claims 1-28, but the Examiner has determined that claims 31-38 and 50-57 should be examined with claims 1-28), classified in class 714, subclass 774.

   II. Claims 29 and 30, drawn to A method of converting a non-interleaving convolutional encoder defined by a reference code of ten or fewer coefficients into an interleaving generalized convolutional encoder, classified in class 714, subclass 786.

   III. Claims 39-49, drawn to A method for interleaving and convolutionally encoding data with a means for performing logic calculations and producing an output based on the performance of the logic calculations, classified in class 714, subclass 752.

   IV. Claims 58-67, drawn to An interleaved generalized convolutional decoder, comprising a metric calculator the metric calculator configured to produce an output based on metrics associated with the encoded input, classified in class 714, subclass 795.

   V. Claims 68-77, drawn to An interleaved generalized convolutional decoder, comprising a subdecoder, classified in class 714, subclass 795.

The inventions are distinct, each from the other because of the following reasons: Inventions Group I and Group II are unrelated. Inventions are unrelated if it can be shown that they are not disclosed as capable of use together and they have different modes of operation, different functions, or different effects (MPEP § 806.04, MPEP § 808.01). In the instant case the different inventions Group II is used in the design of a convolutional encoder and Group II is used for convolutional encoding (Note: design and use are different modes of operation).

Inventions Group I and Group III are unrelated. Inventions are unrelated if it can be shown that they are not disclosed as capable of use together and they have different modes of operation, different functions, or different effects (MPEP § 806.04, MPEP § 808.01). In the instant case the different inventions Group I produces output based on actual calculations whereas Group III produces output based on the performance of logic calculations.

Inventions Group I and Group IV are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention Group I has separate utility such as for encoding. In the instant case, invention Group IV has separate utility such as for decoding. See MPEP § 806.05(d).

Inventions Group I and Group V are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention Group I has separate utility such as for encoding. In the instant case, invention Group V has separate utility such as for decoding. See MPEP § 806.05(d).

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Groups II, III, IV and V, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and the search required for Groups II, III, IV and V is not required for Group I, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art because of their recognized divergent subject matter, restriction for examination purposes as indicated is proper.

During a telephone conversation with Scott Horstemeyer on 11 August 2004 a provisional election was made without traverse to prosecute the invention of Group I, claims 1-28 (Note: The Applicant originally elected claims 1-28, but the Examiner has determined that claims 31-38 and 50-57 should be examined with claims 1-28). Affirmation of this election must be made by applicant in replying to this Office action. Claims 29, 30, 39-49 and 58-77 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Claim Objections

2. Claims 31-38 are objected to because of the following informalities: Nowhere does the Applicant teach a "fifth means for receiving a receiver input". The Examiner assumes the Applicant intended: -- fifth means for receiving a coefficient input -- .Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1, 31 and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda; Yasunari et al. (US 6118825 A, hereafter referred to as Ikeda) in view of Davis; Robert C. (US 4545054 A).

35 U.S.C. 103(a) rejection of claims 1, 31 and 50.

Ikeda teaches a node being capable of receiving a data input (Figure 3 in Ikeda teaches various input notes to Interleaver Circuits 5, 8 and 15), the data input being a portion of a data symbol (in Figure 3 of Ikeda, the input data to any one of the Interleaver Circuits 5, 8 and 15 is a portion of the total data); a memory element, the memory element being capable of storing a plurality of prior data inputs, the prior data inputs being a portion of each of a plurality of prior data symbols (Figure 9 in Ikeda teaches an interleaver for use in Interleaver Circuits 5, 8 and 15, the Interleaver is a memory element, the memory element being capable of storing a plurality of prior data inputs, the prior data inputs being a portion of each of a plurality of prior data symbols), the plurality of prior data inputs being subjected to a variable time delay (in Figure 9 of Ikeda, the time delay for inputs varies depending on switch 31, hence the plurality of prior data inputs being subjected to a variable time delay); and a plurality of logic calculators, the plurality of logic calculators including one or more final logic calculators, the one or more final logic calculators being capable of generating an output, the output being based on the data

input, the plurality of prior data inputs, the plurality of logic calculators, the coefficient input, and the variable time delay (Figure 11 in Ikeda is a convolutional encoder for receiving data from Interleaver Circuits 5, 8 and 15 to convolutionally encode the interleaved input data, the convolutional encoder of Figure 11 has a plurality of logic calculators 67-74, the plurality of logic calculators including one or more final logic calculators 70 and 74, the one or more final logic calculators being capable of generating an output, the output being based on the data input, the plurality of prior data inputs to Interleaver Circuits 5, 8 and 15, the plurality of logic calculators 67-74, and the variable time delay depending on switch 31 in Figure 9 of Ikeda). In addition, the Examiner asserts that one of ordinary skill in the art at the time the invention was made would have known that the various taps to the convolutional encoder of Figure 11 correspond to the coefficients of the generator polynomial for a particular convolutional code, hence the outputs from the convolutional encoder are inherently based on the coefficients of the generator polynomial for the convolutional code represented by the taps connected to logic calculators 67-74.

However Ikeda does not explicitly teach the specific use of a portion of the plurality of logic calculators being capable of receiving a coefficient input.

Davis, in an analogous art, teaches a portion of the plurality of logic calculators being capable of receiving a coefficient input (see Figure 1 in Davis; Note: addition is a binary operation, hence each of the logic calculators 12 and 13 in Figure 1 of Davis are comprised of n adders).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ikeda with the teachings of Davis by including use of a portion of the plurality of logic calculators being capable of receiving a coefficient input. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a portion of the plurality of logic calculators being capable of receiving a coefficient input would have provided the opportunity for adaptive convolutional encoding of input data.

4. Claims 1-7, 10-21, 24-28, 31-35, 38, 50-54 and 57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Herzberg; Hanan (US 5996104 A) in view of Khoury; George (US 5912898 A).

35 U.S.C. 103(a) rejection of claims 1, 16, 31 and 50.

Herzberg teaches; a switch (Serial to Parallel converter 12 in Figure 1 of Herzberg is a switch for directing input to different convolutional encoders); a plurality of convolutional encoders being capable of receiving a data input (Convolutional encoders 14, 16 and 17 in Figure 1 of Herzberg), the data input being a portion of a data symbol, wherein the data input is received by the switch and directed to one of the plurality of convolutional encoders (each of the Convolutional encoders 14, 16 and 17 in Figure 1 of Herzberg receives a portion of the symbols); the plurality of convolutional encoders being capable of storing a plurality of prior data inputs, the prior data inputs for any one of the

convolutional encoders being a portion of each of a plurality of prior data symbols directed to the one of the convolutional encoders, the plurality of prior data inputs being subjected to a unit time delay (of the Convolutional encoders 14, 16 and 17 in Figure 1 of Herzberg is comprised of the convolutional coding circuitry of Figure 4A capable of storing a plurality of prior data inputs in unit delay registers T, the prior data inputs for any one of the convolutional encoders being a portion of each of a plurality of prior data symbols directed to the one of the convolutional encoders, the plurality of prior data inputs being subjected to a unit time delay T); and a plurality of logic calculators associated with each of the plurality of convolutional encoders (the adders in Figure 4A of Herzberg is a plurality of logic calculators associated with each of the plurality of convolutional encoders 14, 16 and 17 in Figure 1 of Herzberg; Note: addition is a binary operation, hence each of the adders in Figure 4A of Davis are comprised of M-1 adders), a portion of the plurality of logic calculators being capable of receiving a coefficient input (encoders (the adders in Figure 4A of Herzberg receive coefficients g_{11}, $g_{12},\ldots,g_{1M}$, g_{21}, $g_{12},\ldots,g_{2M}$), the plurality of logic calculators including at least one final logic calculator, the at least one final logic calculator being capable of producing an output (the adders in Figure 4A of Herzberg inherently include one final logic calculator being capable of producing an output), the output being based on the data input, the plurality of prior data inputs, the plurality of logic calculators and the coefficient input (the output of the adders in Figure 4A of Herzberg is based on the data input, the plurality of prior data inputs, the plurality of logic calculators and the coefficient input).

In addition, Figure 3 of Herzberg teaches interleaver input into the convolutional encoders, but does not teach the details or internal circuitry makeup of the interleavers. However Herzberg does not explicitly teach the specific use of a variable time delay element; wherein the data input is received by the switch and directed to one of the plurality of convolutional encoders based on the variable time delay element.

Khoury, in an analogous art, teaches a convolutional interleaver as required by the Herzberg patent using a variable delay (see Figure 1, Khoury).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Herzberg with the teachings of Khoury by including use of a variable time delay element; wherein the data input is received by the switch and directed to one of the plurality of convolutional encoders based on the variable time delay element. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a variable time delay element; wherein the data input is received by the switch and directed to one of the plurality of convolutional encoders based on the variable time delay element would have provided the opportunity to implement the convolutional interleaver required by the Herzberg patent.

35 U.S.C. 103(a) rejection of claims 2, 17, 32 and 51.

Col. 13, lines 63-67 in Herzberg teach that the data input is a portion of a PAM symbol.

35 U.S.C. 103(a) rejection of claims 3 and 18.

Serial to Parallel converter 12 in Figure 1 of Herzberg is a switch for directing input to different convolutional encoders.

35 U.S.C. 103(a) rejection of claims 4, 19, 33 and 52.

Col. 13, lines 63-67 in Herzberg teach that the data input is a portion of a PAM symbol.

35 U.S.C. 103(a) rejection of claim 5.

Figure 1, Khoury teaches that the variable time delay is a plurality of unit time delays.

35 U.S.C. 103(a) rejection of claims 6, 20, 34 and 53.

Note: the receiving switch for the convolutional encoder in Figure 1 of Khoury sets the delay associated with the variable time delay element.

35 U.S.C. 103(a) rejection of claims 7, 21, 35 and 54.

Note: the receiving switch for the convolutional encoder in Figure 1 of Khoury dynamically sets the delay associated with the variable time delay element.

35 U.S.C. 103(a) rejection of claims 10, 24, 38 and 57.

Line 3 in Figure 1 of Khoury is a 3-unit delay.

35 U.S.C. 103(a) rejection of claims 11 and 25.

Binary multiplication is implemented using AND gates and binary addition using XOR gates, hence AND and XOR gates are the circuit implementation for Figure 4A in Herzberg.

35 U.S.C. 103(a) rejection of claims 12 and 26.

Symbol Selector 16 in Figure 18B is a mapper.

35 U.S.C. 103(a) rejection of claims 13, 14, 27 and 28.

Herzberg and Khoury substantially teaches the claimed invention described in claims1-7, 10-12,16-21 and 24-26 (as rejected above).

However Herzberg and Khoury do not explicitly teach the specific use of software or firmware.

The Examiner asserts that one of ordinary skill in the art at the time the invention was made would have know that firmware and software implementations provide the added benefit of flexibility and scalability.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Herzberg and Khoury by including use of software or firmware. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of software or firmware would have provided the opportunity to implement an alternative embodiment of the teachings in Herzberg and Khoury, which was flexible and scalable.

35 U.S.C. 103(a) rejection of claim 15.

The convolutional encoder of Figure 4A in Herzberg is inherently capable of implementing the specific encoder of the Applicant's claim 15. See In re Swinehart, 439 F.2d 210, 212-13, 169 USPQ 226, 228-29 (CCPA 1971) and In re Schreiber, 128 F.3d 1473, 1477, 44 USPQ2d 1429, 1431 (Fed. Cir. 1997).

5. Claims 8, 9, 22, 23, 36, 37, 55 and 56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Herzberg; Hanan (US 5996104 A) and Khoury; George (US 5912898 A) in view of Ross; Daniel P. (US 4901319 A).

35 U.S.C. 103(a) rejection of claims 8, 22, 36 and 55.

Herzberg and Khoury substantially teaches the claimed invention described in claims 1-7 and 16-21 (as rejected above).

However Herzberg and Khoury do not explicitly teach the specific use of the variable time delay element is based on the quality of a transmission path between a transmitter and the receiver.

Ross, in an analogous art, teaches adaptive interleaving whereby the variable time delay element is based on the quality of a transmission path between a transmitter and the receiver (se Abstract, Ross).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Herzberg and Khoury with the teachings of Ross by

including use of the variable time delay element is based on the quality of a transmission path between a transmitter and the receiver. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of the variable time delay element is based on the quality of a transmission path between a transmitter and the receiver would have provided the opportunity to vary interleaving parameters according to transmission quality.

35 U.S.C. 103(a) rejection of claims 9, 23, 37 and 56.

Fading is a type of noise affecting transmission quality (see Abstract in Ross).

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (703) 308-7066. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Joseph D. Torres, PhD
Art Unit 2133